Serial Number: 09/782,743 Filing Date: February 13, 2001

Filing Date: February 13, 2001 Title: DUAL DOPED GATES

IN THE CLAIMS

- 1. (Previously Presented) A method comprising: preparing a substrate with only PWELLs; and
- forming one or more dual gate structures including NWELLS in the substrate using only one mask.
- 2. (Original) The method of claim 1, wherein preparing a substrate comprises: forming a sacrificial oxide layer on a semiconductor.
- 3. (Previously Presented) The method of claim 1, wherein preparing a substrate with only PWELLS comprises:

forming a gate oxide layer on a semiconductor with only PWELLs; and forming a polysilicon layer on the gate oxide layer.

4. (Original) The method of claim 1, wherein forming one or more dual gate structures in the substrate using only one mask comprises:

forming a first gate structure having a first conductivity in the substrate, the first gate structure being formed using one or more blanket implants; and

forming a second gate structure having a second conductivity in the substrate, the second conductivity having a different value than the first conductivity and the second gate structure being formed using only one masking operation.

5. - 44. (Canceled)

AMENDMENT AND RESPONSE UNDER 37 C.F.R. § 1.116

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45. (Previously Presented) The method of claim 1, preparing the substrate comprises forming a

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PWELL in an n-type substrate.

46. (Previously Presented) The method of claim 1, wherein forming one or more dual gate

structures in the substrate using only one mask comprises forming one or more complementary

metal-oxide semiconductor dual gate structures in the substrate using only one mask.

47. (Previously Presented) The method of claim 2, wherein forming the sacrificial oxide layer

on the semiconductor comprises growing a sacrificial oxide layer to a depth of a few microns.

48. (Previously Presented) The method of claim 3, wherein forming the gate oxide layer on the

semiconductor comprises forming the gate oxide layer having a thickness of between about five

nanometers and about ten nanometers.

49. - 56. (Canceled)

57. (Previously Presented) A method comprising:

preparing a substrate with only NWELLs; and

forming one or more dual gate structures including PWELLS in the substrate using only

one mask.

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58. (Previously Presented) The method of claim 57, wherein preparing a substrate with only NWELLs comprises:

forming a sacrificial oxide layer on a semiconductor.

59. (Previously Presented) The method of claim 57, wherein preparing a substrate with only NWELLs comprises:

forming a gate oxide layer on a semiconductor with only NWELLs; and forming a polysilicon layer on the gate oxide layer.

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